

**AMENDMENTS**

**In the Claims**

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Original) A method for monitoring an execution of a program, the method comprising the steps of:
  - (1) obtaining a first indication including a first address;
  - (2) searching a first memory device for an entry associated with the first address;
  - (3) when the entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device;
  - (4) generating a temporal identifier signal that is associated with the probe signals; and
  - (5) storing the temporal identifier signal and the probe signals in memory.
10. (Original) The method of claim 9,  
step (1) including the step of incrementing a program counter with the first instruction;  
and

step (3) including the step of generating a second probe signal indicating a content of the program counter.

11. (Original) The method of claim 9,  
before step (5),

searching a second memory device for an entry associated with the first address,  
when the entry in the second memory device does not exist, generating at least  
one probe signal indicating a miss entry in the second memory device, and  
generating a temporal identifier signal that is associated with the probe signal.

12. (Original) The method of claim 9,  
before step (2),

searching an address storage device for an entry associated with the first address,  
when the entry in the address storage device does not exist, generating at least one  
probe signal indicating a miss entry in the address storage memory device,  
and  
generating a temporal identifier signal that is associated with the probe signal.

Please add the following new claims:

12. 13. (Currently Amended) A method for monitoring an execution behavior of a  
program, comprising:

generating probe signals representative of memory access misses occurring in a  
processor;  
receiving the probe signals and associating a temporal identifier signal with the probe  
signals; and  
storing the temporal identifier signal and the probe signals; and  
generating a second high-speed memory miss signal, a second high-speed memory miss  
count signal and a time stamp signal, the second high-speed memory miss signal  
indicating a miss in a second high-speed memory, the second high-speed memory  
miss count signal representing a number of misses in the second high-speed

memory, and the time stamp signal indicating when the second high-speed memory miss signal is active.

14. (New) The method of claim 13, further comprising:  
generating probe signals in response to a memory access miss signal when executing a specified instruction.
15. (New) The method of claim 13, further comprising:  
generating probe signals recording a TLB miss when executing a specified instruction.
16. (New) The method of claim 13, further comprising  
generating a program counter signal, a TLB identification signal indicating a miss in the TLB, a TLB miss count signal representing an accumulative count of TLB misses, and a time stamp signal when the TLB miss signal is activated.
17. (New) The method of claim 16, further comprising  
incrementing a TLB miss counter when the TLB miss signal is activated.
18. (New) The method of claim 13, wherein  
the program executes on a processor;  
the processor includes a first high-speed memory and a program counter, the first high-speed memory generating a first high-speed memory miss signal; and  
a probe logic unit generates a program counter signal, a first high-speed memory miss signal indicating a miss in the first high-speed memory, a first high-speed memory miss count signal representing a number of misses in the first high-speed memory, and a time stamp signal when the first high-speed memory miss signal is activated.
19. (New) The method of claim 18, wherein  
the probe logic unit includes a first high-speed memory miss counter coupled to the first high-speed memory miss signal, the first high-speed memory miss counter is incremented when the first high-speed memory miss signal is activated.